EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Tushar Parlikar, Reg.# 61,715 on 05/13/2010.

3. <u>This listing of claims will replace all prior versions and listings of claims in the application:</u>

1 – 53. (Canceled).

54. (Currently Amended) A method for dynamic slip control in a scheduling system, the method comprising:

a processor receiving a first interrupt;

the processor retrieving from a memory a value of a first clock time when the first interrupt is received;

<u>the processor computing an estimated scheduled time interval to a second interrupt;</u>

<u>the processor retrieving from the memory a value of a second clock time when</u>

computation of the estimated scheduled time interval is complete;

the processor computing a first time interval between said first clock time value and [[a]] the estimated scheduled time interval ~~for a~~ to the second interrupt;

~~the processor retrieving from the memory a value of a second clock time when computation of the first time interval is complete;~~

the processor computing a second time interval between said first clock time value and said second clock time value;

the processor computing a ~~third~~ revised scheduled time interval by subtracting said second time interval from said first time interval; and

the processor scheduling said second interrupt to arrive at or after an expiration of said ~~third~~ revised scheduled time interval.

55. (Previously Presented) A method according to claim 54, further comprising: after the act of obtaining the value of a first clock time when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete, updating a state variable of said scheduling system.

56. (Previously Presented) A method according to claim 54, further comprising: after the act of obtaining the value of a first clock time when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete, interacting with a physical environment via an interface circuit.

57. (Previously Presented) A method according to claim 56, wherein said act of interacting with the physical environment comprises receiving a signal from the physical environment indicative of a state of the physical environment.

58. (Previously Presented) A method according to claim 56, wherein said act of interacting with the physical environment comprises receiving an instruction from the physical environment to modify a state of the scheduling system.

59. (Currently Amended) A method according to claim 54, further comprising estimating a latency of receipt of said first interrupt, and wherein said act of computing said second and said ~~third~~ revised scheduled time intervals is further based on said estimated latency.

60. (Previously Presented) A method according to claim 59, wherein said first interrupt is received from a first platform and the act of estimating said latency comprises analyzing a performance characteristic of said platform.

61. (Previously Presented) A method according to claim 59, wherein said first interrupt is received from a first platform and the act of estimating said latency comprises accessing statistical information regarding a performance characteristic of said platform.

62. (Currently Amended) A method according to claim 54, further comprising estimating a processing time for updating a state of said scheduling system, and wherein said act of computing said second and said ~~third~~ revised scheduled time intervals is further based on said estimated time.

63. (Previously Presented) A method according to claim 62, wherein the act of estimating said processing time comprises analyzing a performance characteristic of said scheduling system.

64. (Previously Presented) A method according to claim 62, wherein the act of estimating said processing time comprises accessing statistical information regarding a performance characteristic of said scheduling system.

65. (Currently Amended) A computer program product for use with a scheduling system comprising a computer readable medium encoded with a program module, the program module including instructions for directing the scheduling system to:

receive a first interrupt;

obtain a value of a first clock time when the first interrupt is received;

compute an estimated scheduled time interval to a second interrupt;

obtain a value of a second clock time when computation of the estimated scheduled time interval is complete;

compute a first time interval between said first clock time value and [[a]] the

estimated scheduled time interval ~~for a~~ to the second interrupt;

~~obtain a value of a second clock time when computation of the first time interval is complete;~~

compute a second time interval between said first clock time value and said second clock time value;

compute a ~~third~~ revised scheduled time interval by subtracting said second time interval from said first time interval; and

schedule said second interrupt to arrive at or after an expiration of said ~~third~~ revised scheduled time interval.

66. (Previously Presented) A computer program product according to claim 65, wherein the program module further includes instructions directing the scheduling system to update a state variable of said scheduling system after the act of obtaining the value of a first clock time when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete.

67. (Previously Presented) A computer program product according to claim 65, wherein the program module further includes instructions directing the scheduling system to interact with a physical environment via an interface circuit after the act of obtaining the value of a first clock time when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete.

68. (Previously Presented) A computer program product according to claim 67, wherein said instructions directing the scheduling system to interact with the physical environment comprise instructions directing the scheduling system to receive a signal from the physical environment indicative of a state of the physical environment.

69. (Previously Presented) A computer program product according to claim 67, wherein said instructions directing the scheduling system to interact with the physical environment comprise instructions directing the scheduling system to receive an instruction from the physical environment to modify a state of the scheduling system.

70. (Currently Amended) A computer program product according to claim 65, wherein the program module further includes instructions directing said scheduling system to estimate a latency of receipt of said first interrupt, and wherein said instructions directing the scheduling system to compute said second and said ~~third~~ revised scheduled time intervals further include instructions to compute said second time interval based on said estimated latency.

71. (Previously Presented) A computer program product according to claim 70, wherein said first interrupt is received from a first platform and the instructions directing said scheduling system to estimate said latency comprise instructions directing said scheduling system to analyze a performance characteristic of said platform.

72. (Previously Presented) A computer program product according to claim 70, wherein said first interrupt is received from a first platform and the instructions directing said scheduling system to estimate said latency comprise instructions directing said scheduling system to access statistical information regarding a performance characteristic of said platform.

73. (Currently Amended) A computer program product according to claim 65, wherein the program module further comprises instructions directing the scheduling system to estimate a processing time for updating a state of said scheduling system, and wherein said instructions directing the scheduling system to compute said second time interval further include instructions to computer said second and said ~~third~~ revised scheduled time intervals based on said estimated time.

74. (Previously Presented) A computer program product according to claim 73, wherein the instructions directing the scheduling system to estimate said processing time include instructions directing the scheduling system to analyze a performance characteristic of said scheduling system.

75. (Previously Presented) A computer program product according to claim 73, wherein the instructions directing the scheduling system to estimate said processing time

comprise instructions directing the scheduling system to access statistical information regarding a performance characteristic of said scheduling system.

76. (Currently Amended) A scheduling system employing dynamic slip control, the scheduling system

comprising:

at least one input ~~adapted~~ configured to receive an interrupt;

at least one timer circuit; and

a processor coupled to said timer circuit and said input, the processor ~~adapted~~ configured to obtain

a value of a first clock time when a first interrupt is received, compute an estimated scheduled time interval to a second interrupt, obtain a value of a second clock time when computation of the estimated scheduled time interval is complete, compute a first time interval between said first clock time value and [[a]] the estimated scheduled time interval ~~for a~~ to the second interrupt, ~~obtain a value of a second clock time when computation of the first time interval is complete,~~ compute a second time interval between said first clock time value and said second clock time value, compute a ~~third~~ revised scheduled time interval by subtracting said second time interval from said first time interval, and schedule said second interrupt to arrive at or after an expiration of said ~~third~~ revised scheduled time interval.

77. (Currently Amended) A system according to claim 76, wherein the processor is further ~~adapted~~ configured to update a state variable of said scheduling system after the act of obtaining the value of a first clock when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete.

78. (Currently Amended) A system according to claim 76, further comprising a physical environment coupled to said processor and wherein the processor is further ~~adapted~~ configured to interact with the physical environment via an interface circuit after the act of obtaining the value of a first clock time when the first interrupt is received and before the act of obtaining the value of a second clock time when computation of the first time interval is complete.

79. (Currently Amended) A system according to claim 78, wherein the processor is further ~~adapted~~ configured to receive a signal from the physical environment indicative of a state of the physical environment.

80. (Currently Amended) A system according to claim 78, wherein the processor is further ~~adapted~~ configured to receive an instruction from the physical environment to modify a state of the scheduling system.

81. (Currently Amended) A system according to claim 76, wherein the processor is further ~~adapted~~ configured to estimate a latency of receipt of said first interrupt, and compute said second and said ~~third~~ revised scheduled time intervals based further on said estimated latency.

82. (Currently Amended) A system according to claim 81, further comprising a platform ~~adapted~~ configured to send said first interrupt, said processor further ~~adapted~~ configured to analyze a performance characteristic of said platform.

83. (Currently Amended) A system according to claim 81, further comprising a platform ~~adapted~~ configured to send said first interrupt, said processor further ~~adapted~~ configured to access statistical information regarding a performance characteristic of said platform.

84. (Currently Amended) A system according to claim 76, wherein the processor is further ~~adapted~~ configured to estimate a processing time for updating a state of said scheduling system, and compute said second and said ~~third~~ revised scheduled time intervals based further on said estimated time.

85. (Currently Amended) A system according to claim 84, said processor further ~~adapted~~ configured to analyze a performance characteristic of said scheduling system.

86. (Currently Amended) A system according to claim 84, said processor further ~~adapted~~ configured to access statistical information regarding a performance characteristic of said scheduling system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Abdullah-Al Kawsar/
Examiner, Art Unit 2195